C. Byregowda Institute of Technology, KOLAR

First /Second Semester B.E. Degree Examination, Model paper-1

Basic Electronics (15ELN 15/25) Solutions

Module-l

1.a Define the following parameters:

i) PIV ii) Knee voltage iii) Dynamic resistance (6 marks)

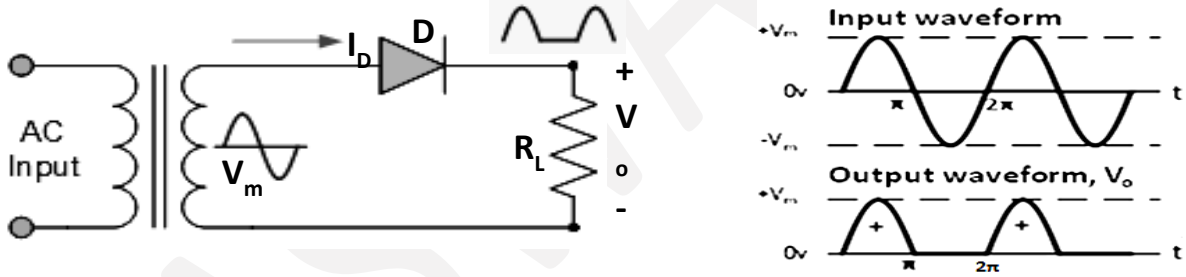
i) PIV: (Peak Inverse Voltage) : It is a maximum reverse voltage that a diode can withstand without damage, measured in volts.

ii) Knee Voltage (V_k) : The voltage at which the diode forward current (I_F) increases rapidly, measured in milli amps (mA).

iii) Dynamic resistance (r_d) : It is the ratio of $\frac{\text{small change in diode forward voltage}}{\text{respective change in its forward current}}$ measured in ohms (Ω).

1.b With neat circuit diagram and waveforms, explain the working of half wave rectifier (6 marks)

Half wave rectification is used to convert AC into rippled DC, carried out by a single diode and its arrangement is as shown in the below fig.



During **positive half cycle** of the secondary voltage V_m:

- Diode is forward biased, acts like a closed switch.
- It offers low resistance R_F, hence, it conducts for $0 \le t \le \pi$. See fig. 9(b).
- Then, diode current I_D flows through the load resistance R_L. Therefore, output voltage $V_o = I_D R_L$.

During **negative half cycle** of the secondary voltage V_m:

- Diode is reverse biased, acts like a open switch.
- It offers very high resistance R_r, hence, it does not conduct for $\pi \le t \le 2\pi$.
- Then, diode current $I_D = 0$. Therefore, output voltage $V_o = 0$.

The cycle repeats. Input-output voltage wave forms are as shown in the fig. 9(b).

A half wave rectifier is rarely used in practice, because it conducts only for positive half cycle of the input. It is never preferred as the power supply of an audio circuit due to its high ripple factor.

1.c Draw CE circuit and sketch the I/O characteristics. Also explain operating regions by indicating them on the characteristics curve. (4 marks)

In CE configuration, the Emitter terminal is connected as a common terminal. The input is applied between the Base and Emitter terminals. The output is taken between the Collector and Emitter terminals.

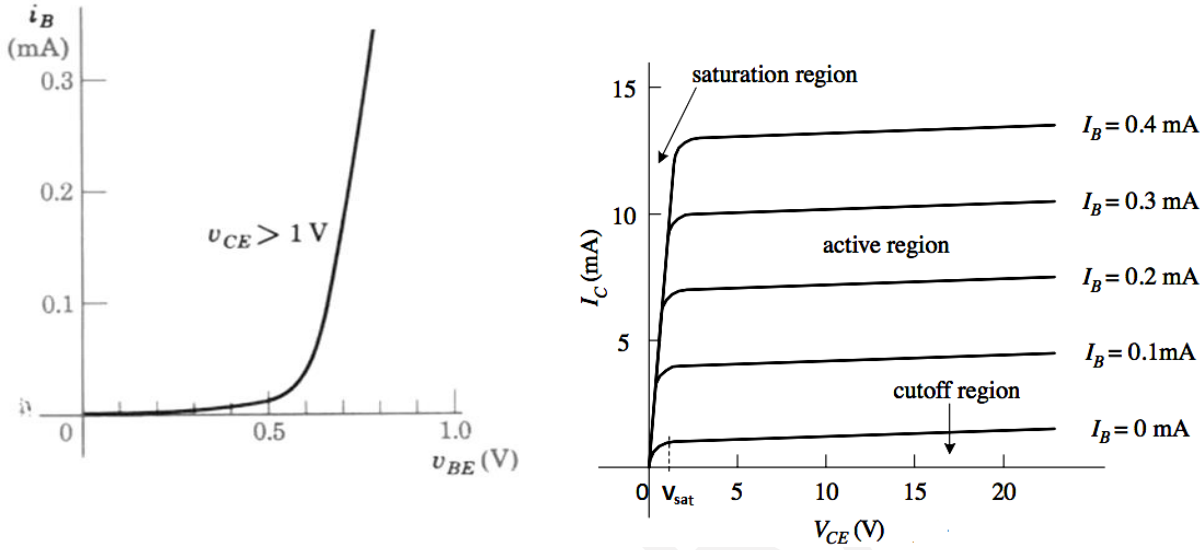
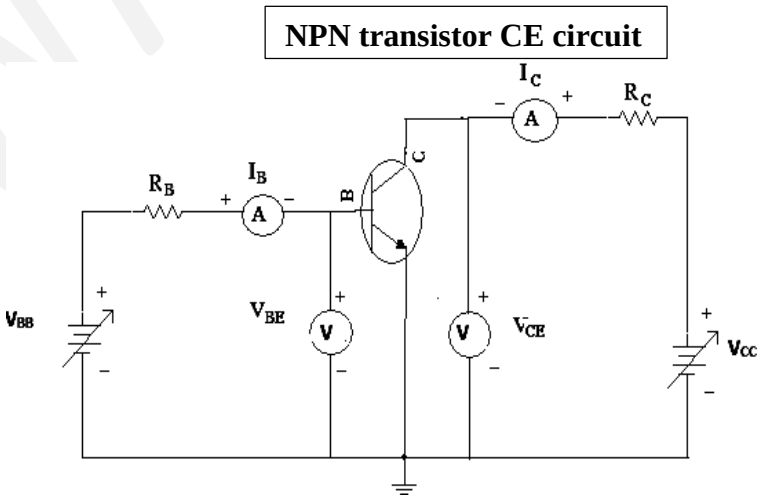


Fig. NPN transistor CE configuration: (a) Input characteristics (b) output characteristics

Observations and analysis from output characteristics: see the fig. (b)

There are *three regions* observed:



(i) **Cut-off region** (the curve below $I_B \cong 0$):

- J_{BE} and J_{CB} junctions of transistor are reverse biased.
- Hence the transistor acts as open switch, because, $I_C \cong I_E \cong 0$. But due to minority carriers $I_C = I_{CEO}$.

(ii) **Saturation region** –

- This is the region of characteristics at origin in which J_{BE} and J_{CB} junctions of transistor are forward biased. I_C increase exponentially with $V_{CE\,(sat)}$. Hence the transistor acts as closed switch.

Between cut-off and saturation regions normally transistor is employed for digital switch.

(iii) **Active-region** –

- Defined as region of characteristics right of $V_{CE\ (sat)}$, in which J_{BE} and J_{CB} junctions of transistor are forward and reversed biased, respectively. I_C becomes slightly constant for each level of I_B. This shows I_C depends more on each level of I_B and less dependent on V_{CE}.
- For large variation in V_{CE} small I_C increases. The slope of lines represents the output resistance $R_{out} = \frac{\Delta V_{CE}}{\Delta I_C}\ \Omega$ (when I_B constant).

Active region is normally employed for linear amplification.

2. a Explain zener diode regulator circuit with no load and with load. (6 marks)

The circuit diagram of the zener diode as a simple voltage regulator is shown in fig. The resistor, R_S is connected in the circuit to limit the current flow through the zener diode with the input voltage source, V_{in}. The stabilized output voltage V_o (= V_z) is taken from across the zener diode. The zener diode is operating in the breakdown region when it is reverse biased by connecting with its cathode terminal to the positive of the supply V_{in}.

- As long as $V_{in} > V_Z$, the zener diode operates in the breakdown region and maintains constant voltage across the load, irrespective changes in load current or input voltage.

Case 1) : Under No load condition

- No R_L is connected across the load, hence, $I_L = 0$
- I_S passes through R_S and the zener diode which in turn dissipates its maximum power, measured as $P_{D\ (max)} = V_Z\ I_{z\ (max)}$
- Zener diode works as voltage regulator as long as $I_z < I_{z\ (max)}$.

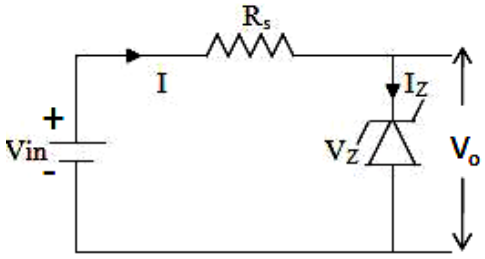


Fig. **No load condition**

Case 2) : Under load condition

- R_S and R_L are fixed
- Only input voltage V_{in} (> desired V_o) is varied
- As current I varies, the voltage drop across R_S and I_z varies, but output voltage ($V_o = V_z$) would remain constant as long as V_{in} is maintained above a minimum value. i.e., $V_o = Vin - I\ R_S$

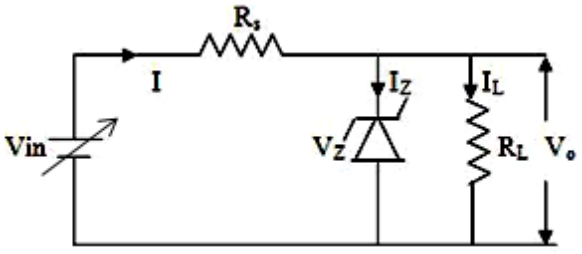


Fig. **load condition**

2. b Input to the full wave rectifier is *v* = 200 sin 50t volts, if load resistance is 1 K Ω and forward resistance is 50 Ω. Find:

(i) DC current through the circuit

(ii) AC(rms) value of current

(iv) **DC output voltage,**

(v) **AC power input**

(vi) **DC power output**

(vii) **Rectifier efficiency.** **(6 marks)**

Solution: Given $V_m = 200$ V

$R_L = 1$ K Ω,

$R_F = 50$ Ω (for each diode)

To find I_m : $I_m = \frac{V_m}{R_L + R_F} = \frac{200}{(1000+50)} =$ **0.19A**

(i) DC (Load) current, $I_L = \frac{2I_m}{\pi} = \frac{2 \times 0.19}{\pi} =$ **0.121 A**

(ii) RMS current $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{0.19A}{\sqrt{2}} =$ **0.134A**

(iii) DC Output voltage, $V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 200}{\pi} =$ **127.32 V**

(iv) Ac Power $= I^2(rms)(R_L + R_F) = 0.134^2 \times (1000+50) =$ **18.85 W**

(v) DC Power $= I^2(Load)(R_L) = 0.121^2 \times 1000 =$ **14.64 W**

(vi) Rectifier Efficiency $\eta = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_L + R_F)} \times 100\%$

$\eta = \frac{14.64}{18.85} \times 100\% =$ **77.66%**

2.c. Derive the relationship α and β. Calculate the value of I_C, I_E for a transistor that has α = 0.98 and I_B =100μA. **(4 marks)**

We know that, α is current amplification gain in CB transistor defined as $\alpha = \frac{I_C}{I_E}$ …….. (1)

β is current amplification gain in CE transistor, defined as $\beta = \frac{I_C}{I_B}$ …….. (2)

Transistor total current equation $I_E = I_B + I_C$ …… (3)

Divide eqn (3) both sides by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C} \quad \text{……} \quad (4)$$

using eqn (1) and eqn (2)

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \text{……} \quad (5)$$

Solving for α and β by using eqn (5) $\alpha = \frac{\beta}{(\beta+1)}$ …… (6)

$$\beta = \frac{\alpha}{(1-\alpha)} \qquad \text{..... (7)}$$

Solution: Given, $\alpha = 0.98$ and $I_B = 100\mu A$.

We know that, $\beta = \frac{\alpha}{(1-\alpha)} = 0.98 / (1 - 0.98) = \mathbf{49}$

$I_C = \beta I_B = 49 \times 100 \times 10^{-3} = \mathbf{4.9\ mA}$

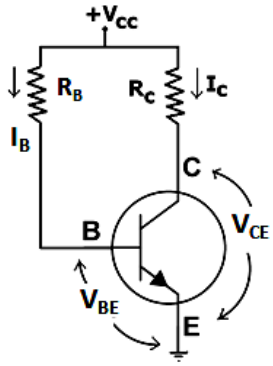
$I_E = I_B + I_C = 100 \times 10^{-6} + 4.9 \times 10^{-3} = \mathbf{4.91\ mA}$

Module 2

3.a What is a DC load line ? Explain base biased method with necessary equations. (5 marks)

The *dc load line* is the straight line joining by the locus of I_C and V_{CE} at which the transistor remains in active region.

- Assuming a constant value for V_{BE}, we can solve for both I_B and I_C and determine the output voltage V_{CE} of the transistor.
- In the base bias method a single voltage source V_{CC} is applied to the Collector and Base of the transistor using R_B and R_C resistors. The circuit shown in the fig. 3 is called as a fixed bias circuit.



Q-point coordinates of Fixed Bias circuit	
$I_{CQ} = \beta [(V_{CC} - V_{BE}) / R_B]$	$V_{CEQ} = V_{CC} - I_C R_C$

- In this method the transistor base current I_B remains constant for given values of V_{CC} and R_B. Therefore, Q- point of the transistor remains fixed. The selection of R_B sets the level of I_B so that the Q – point can be adjusted. The value of R_B is calculated by: $R_B = \frac{V_{CC} - V_{BE}}{I_B}$ where I_B is defined as I_C / β.
- This type of biasing is β dependent. Where, β of a transistor is unstable and unpredictable parameter of a transistor, because, β is a function of temperature.

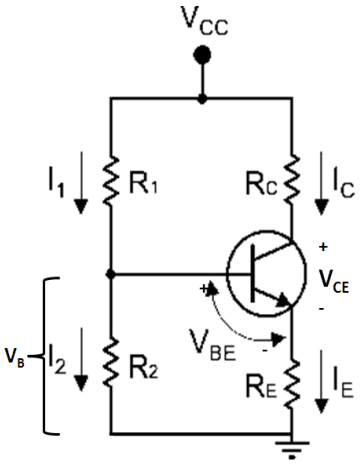
3.b. Explain the characteristics of ideal Opamp. Mention two applications of Opamp. (6Marks)

The main applications of op-amp: Active filters, oscillators, peak detector, comparators, voltage regulators, precision rectifiers, instrumentation and control systems, pulse generators, square wave generators etc.

Op amp Characteristics	Ideal	Practical
1. Open-loop voltage gain: $A_{OL} = V_o/ (V_1 – V_2)$: The ratio of output voltage to difference in the input voltage when there are no external feedback components.	∞	**2 x 10^5**
2. Common-Mode Rejection Ratio: $\text{CMRR} = \frac{A_d}{A_c} = 20\log_{10}\frac{A_d}{A_c}(\text{dB})$ The measure of an amplifier's ability to reject common-mode signals. It is defined as the ratio of differential gain to the common mode gain, measured in dB.	∞	**90 B**
3. Slew Rate $S_R = dV_{o\,(max)}/dt$: It describes how fast the output voltage responds to an immediate change in input voltage. It is defined as the rate of change of maximum output voltage with respect to time. The higher the value (in V/μs) of slew rate, the faster the op-amp responds.	∞	**0.5 V/μs**
4. Bandwidth: The range of frequencies (from DC to the highest AC) that the op-amp amplifies for a given gain. In real op-amps, the bandwidth is rather limited. This limitation is specified by the Gain-Bandwidth product (GB).	∞	**1 M Hz**
5. Input Resistance: R_i : This is the resistance looking into the input terminals with the op-amp operating without feedback (open loop). The larger the resistance of a device, the smaller the current that it demands.	∞	**2M Ω**
6. Output Resistance: R_o : Resistance measured at the output terminal with respect to the ground. The high impedance ensures that op-amp draws very little current and does not cause any loading issue in the circuit.	**0**	**75 Ω**
7. Input Off-Set Voltage (V_{ios}): The ideal OP-AMP produces zero output for zero input. A practical op-amp, however, has a small DC voltage at the output, when its differential input is zero. The input offset voltage is the small inputs that is necessary to make output Vo = 0.	**0**	**2 m V**
8. Input Offset Current (I_{ios}): Ideally, the two input bias currents are equal but in practical op-amps the bias currents are not exactly equal. I_{OS}: $I_{OS} = \lvert I_1 - I_2 \rvert$	**0**	**20 n A**
9. Input Bias Current: The input bias current is the DC current required by the inputs of the amplifier to properly operate the first stage.	**0**	**80 n A**
10. Power Supply Rejection Ratio (PSRR): The output of an op-amp is to be independent from its power supply. Every real op-amp has a finite PSRR that reflects how well the it can reject the changes in its supply voltage. $\text{PSRR} = \Delta V_{ios}/\Delta V_{CC}$ at V_{EE} constant or $\text{PSRR} = \Delta V_{ios}/\Delta V_{EE}$ at V_{CC} constant	**0**	**30 μV/V**

3.c With neat circuit diagram, explain voltage divider bias circuit using approximate analysis. (5 marks)

- Voltage divider bias is the most popular bias technique which provides high bias stability.
- In the circuit shown in the fig.4, R_1 and R_2 divide the supply voltage V_{CC} and hence it is called as Voltage divider circuit.
- Voltage across R_2 provides a fixed bias voltage V_B at the transistor Base that fixes V_{BE} and so it is possible to produce and control the I_C using the base current I_B.
- The net forward bias $V_{BE} = V_B - V_E$ (= voltage drop across R_E).
- Resistance R_E is connected in series with the Emitter that provides the stabilization. Since, the base current I_B is very much smaller than the current I_2, through R_2, the base voltage V_B remains practically unchanged.
- This bias technique is independent of β and V_{BE} variations.



Assumption: The Base current I_B is very much smaller than the current I_2, through the resistor R_2.

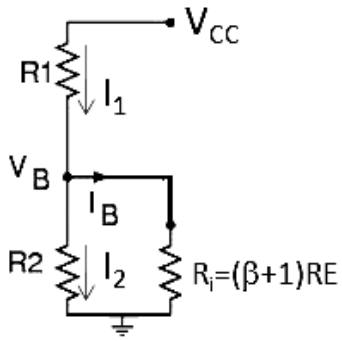


Fig.1 Equivalent circuit for input resistance R_i

As seen in the fig. 1, R_i is the equivalent resistance between Base and the ground with an emitter resistor R_E, is seen as $(\beta+1)R_E$

Proof:

$$V_E = I_E R_E \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

where, $I_E = I_C + I_B$, but $I_C = \beta I_B$

$I_E = \beta I_B + I_B = (\beta+1) I_B$ then, eqn (1) becomes

$$V_E = (\beta+1) I_B R_E \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

$$R_i = V_E / I_B = (\beta+1)R_E \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

or $$\mathbf{R_i = (\beta+1) R_E \geq 10R_2}$$

- Since, $\beta >> 1$, $R_i >> R_2$, then the current $I_B << I_2$. This makes I_B to be negligible.
- Thus $I_1 \cong I_2$. Therefore, R_1 and R_2 can be considered as in series.
- Voltage divider can be applied to find the voltage across R_2 (= V_B)

$$\mathbf{V_B = V_{CC}\, R_2 / (R_1 + R_2)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

- Once V_B is determined, V_E is calculated as, $V_E = V_B - V_{BE}$

  After finding V_E, I_E is calculated as, $I_E = V_E / R_E$, $I_E \cong I_C$ (I_B to be negligible),

$$\mathbf{I_{CQ} \approx I_E = V_E / R_E} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

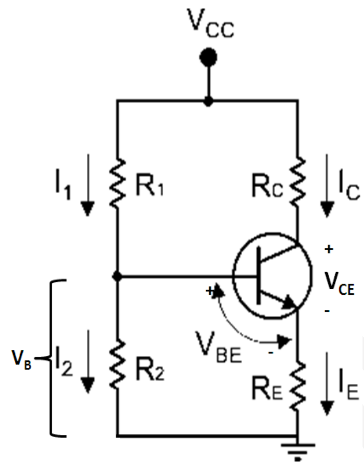
- Level of V_{CE} is determined by applying KVL to the Collector - Emitter loop.

  Taking $I_E \cong I_C$ $$\mathbf{V_{CE} = V_{CC} - I_C (R_C + R_E)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

Note that in the above derivations, β is not involved and I_B is not calculated. That means, the Q-point (I_{CQ} and V_{CEQ}) is therefore independent of the value β.

4. a. Design the voltage divider bias circuit to operate from 12V supply. The bias conditions are V_{CE} = 3V, V_E = 5V, and I_C = 1mA. (5 marks)

Solution: Given, V_{CC} = 12V , V_{CE} = 3V, V_E = 5V, and I_C = 1mA



i) **To find R_C:** Applying KVL to the outer loop, we get, $V_{CC} = I_C R_C + V_{CE} + V_E$

$12 = 1x\ 10^{-3} R_C + 3 + 5$

$R_C = 12 – 8 / 1x\ 10^{-3}$ = **4 KΩ**

ii) **To find R_E:** $V_E = I_E R_E$ (Taking $I_E \cong I_C$)

$R_E = V_E / I_E = 5 / 1x\ 10^{-3}$ = **5 KΩ**

iii) **To find R_2:** By thumb rule, $I_2 \cong I_C / 10$

$I_2 \cong 1x\ 10^{-3} / 10$ = **0.1mA**

$V_B = V_{BE} + V_E = 0.7 + 5$ = **5.7V**

Also, $V_B = I_2 R_2$

∴ $R_2 = V_B / I_2 = 5.7 / 0.1\ x10^{-3}$ = **57 KΩ**

iv) **To find R_1:** Using voltage divider rule

$V_B = V_{CC} \cdot R_2 / (R_1 + R_2)$

$5.7 = 12 \cdot 57\ x\ 10^3 (R_1 + 57\ x\ 10^3)$

∴ R_1 = **63 KΩ**

4. b Derive an expression for 3 input summing amplifier. (5 marks)

- The inverting summing or adder op-amp circuit for three inputs is shown in the fig. The output voltage, (Vo) is proportional to the algebraic sum of the input voltages, V_1, V_2, V_3. Because effectively it adds individual input voltage signals.

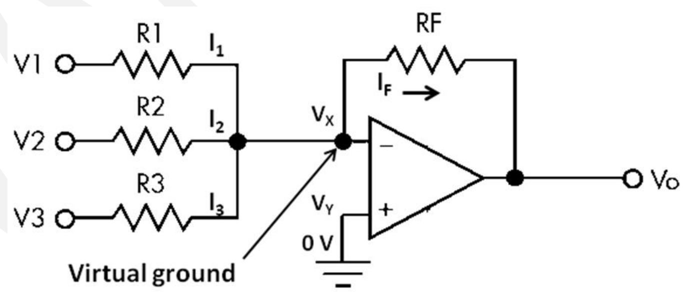


Fig. Inverting summing op-amp circuit

- Input signals V_1, V_2 and V_3 are applied to the inverting (-) input of the op-amp through input resistors R_1, R_2 and R_3, respectively. Thus, I_1, I_2 and I_3 are input currents flow through them.
- R_F is connected between the V_o and the (-) input. The non-inverting input is connected to ground.

Virtual ground concept:

- 1. No input current flows into the (-) terminal and
- 2. V_X always equals V_Y. Therefore, all input currents flow towards output (V_{out}) through R_F.

Analysis: Apply KCL at node V_X, using nodal analysis in the direction of current flow,

$$I_1 + I_2 + I_3 = I_F \quad \ldots\ldots (1)$$

Where, $I_1 = \frac{V_1 - V_X}{R_1}$, $I_2 = \frac{V_2 - V_X}{R_2}$, $I_3 = \frac{V_3 - V_X}{R_3}$ and $I_F = \frac{V_X - V_o}{R_F}$

Then eqn (1) becomes,

$$\frac{V_1 - V_X}{R_1} + \frac{V_2 - V_X}{R_2} + \frac{V_3 - V_X}{R_3} = \frac{V_X - V_o}{R_F} \quad \text{since,} \quad V_X = V_Y = 0$$

$$\frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} + \frac{V_3 - 0}{R_3} = \frac{0 - V_o}{R_F}$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_o}{R_F}$$

$$V_o = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right] \qquad \text{if } R_1 = R_2 = R_3 = R_F = R$$

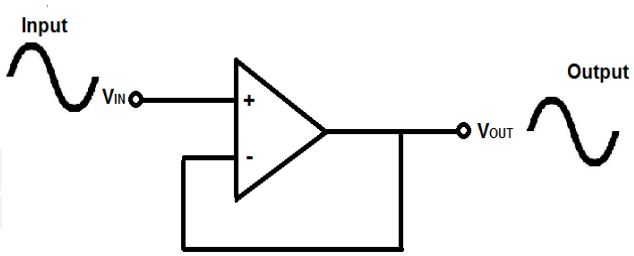
$V_o = -(V_1 + V_2 + V_3)$

≡ output voltage is proportional to the algebraic sum of the input voltages, V_1, V_2, V_3.

4. c Explain Voltage follower with neat circuit and necessary equations. (5 marks)

Output voltage V_{out} follows the input voltage V_{in} so the circuit is named as op-amp voltage follower.

The output is connected directly back to the (-) inverting input so that the feedback is 100% and V_{in} is exactly equal to V_{out}. It is shown in the fig.



- If voltage V_{in} increases, voltage V_{out} increases. On the other hand, if voltage V_{in} decreases, voltage V_{out} also decreases.
- It provides an effective isolation of the output from the signal source that eliminating the loading effect of the second circuit from the first circuit. Because the input impedance of the op amp is very high, draws very little power from the signal source, avoiding loading effects. This circuit is useful for the first stage.

Properties of voltage follower:

- Voltage gain = 1
- Input impedance $R_{in} = \infty$
- Output impedance $R_{out} = 0$
- Effective isolation of the output from the signal source.

To Prove Voltage gain, $\frac{V_{out}}{V_{in}} = A_V = 1$

Voltage follower is resembles to that of non-inverting opamp, in which input impedance R_{in} is open circuited (= ∞) and output impedance R_{out} is short circuited (= 0). See fig. 16(b).

$$\frac{V_{out}}{V_{in}} = A_V = \left[\frac{R_F}{R_1} + 1\right] \quad \rightarrow \quad \frac{V_{out}}{V_{in}} = A_V = \left[\frac{0}{\infty} + 1\right] = 1$$

Applications: The voltage follower is often used as buffers for logic circuits, impedance matching.

Advantage: provides current and power gain.